REMARKS/ARGUMENTS

This is in response to the Office Action dated October 23, 2009. Claims 1-6, 8 and 10-11 are pending and stand rejected in the outstanding Office Action. Claim 6 has been amended.

The rejection of independent claim 1, as allegedly being anticipated under 35 U.S.C. § 102(b) by Nakai et al. (US 6,207,890) is respectfully traversed. Nakai fails to disclose or even remotely suggest each and every limitation set forth in the claims. Anticipation requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference", *Verdegaal Bro. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987) (MPEP § 2131).

The Examiner identified the intrinsic amorphous silicon layer 2 (see Fig. 11 in Nakai) as the claimed first conductivity type semiconductor layer, identified the p-type amorphous silicon layer 3 as the claimed second conductivity type semiconductor layer, and identified the front electrode 4 as the claimed front electrode being in direct physical contact with the second conductivity type layer 3. Moreover, according to the Examiner, claim 1 is a product-by-process claim, therefore no patentable weight was given to the limitation "by implanting second conductivity type impurities into the surface of the first conductivity type semiconductor substrate. Finally, the Examiner asserted that "although the claim requires a partial direct physical contact between the front electrode and the second conductivity type semiconductor layer, the claim does not preclude the layers being in full contact, and therefore the claim is anticipated", see p. 3 of the Office Action.

The Examiner is incorrect in making the above assertion. Partial excludes full. Construction of the term "partial" under plain language clearly excludes an interpretation that includes a "full" or "total" feature. Webster's Collegiate Dictionary provides the following

definition for "partial", "of or relating to a part rather the whole: not general or total", emphasis added. Fig. 11 of Nakai shows that electrode 4 is in complete/full contact with layer 3.

The rejection of claim 1 under 35 U.S.C. §103(a), as allegedly being unpatentable over Nakai in view of Tsuzuki et al. (US 6,184,457), is respectfully traversed.

The Examiner identified layer 2 in Fig. 11 of Nakai as the claimed first conductivity type semiconductor layer, identified layer 3 as the claimed second conductivity type semiconductor layer, and identified electrode 5 as the claimed front electrode, allegedly being in partial contact with layer 3. The Examiner asserted again that claim 1 is a product-by-process claim. Moreover, the Examiner stated that "although Nakai shows that the comb-like collecting electrode 5 is in partial contact with the layer 3, the reference is silent as to direct physical contact", and turned to Tsuzuki for the missing limitation, see p. 5 of the Office Action.

Tsuzuki discloses a solar cell (Fig. 9), wherein layers 801 and 802 comprise a p-n junction, and 804 is a collector electrode. According to the Examiner, collector electrode 804 is partially in direct physical contact with the layer 802, hence it would have been obvious to have made the electrode 5 of Nakai partially in direct physical contact with the layer 3 of Nakai, as taught by Tsuzuki, see p. 6 of the Office Action.

First, unlike the Examiner's assertion, layer 3 in Nakai is not in partially contact with the collecting electrode 5. Instead, there is complete separation between layer 3 and electrode 5, provided by the intervening layer 4. Second, the Examiner, has not specified how exactly to modify Nakai in view of Tsuzuki to arrive at the claimed structure. In Nakai, there exists layer 4 which covers completely layer 3 and is between layer 3 and electrode 5. The Examiner has not said what to do with layer 4 that exists in Nakai and acts as a front electrode, if the structure of

Tsuzuki were to be adopted, i.e., a structure that does not include an intervening layer between the semiconductor layer and the comb-like electrode.

In Nakai, a collecting electrode 5 (corresponding to "front electrode 8" of the invention of claim 1) does not physically contact with a p-type amorphous silicon layer 3 (corresponding to "second conductivity type semiconductor layer 5 of the invention of claim 1) due to the front electrode 4 (which is deemed to be an essential element of Nakai) interposed therebetween (see Fig. 11). Therefore, there is no point in replacing the collecting electrode 5 with a collector electrode 804 of Tsuzuki.

Moreover, a semiconductor layer of Nakai comprises three layers, i.e., a p-type amorphous silicon layer 3 (hereinafter referred to as "p-type layer 3"), an intrinsic amorphous silicon layer 2 (i.e., i-type layer), and an n-type single crystalline silicon substrate 1 (i.e., n-type layer), laminated in this order from a side that receives light. These three layers thus constitute a p-i-n junction structure.

It is deemed that the semiconductor layer of Nakai has the front electrode on the light-receiving side by necessity. Namely, it is necessary for Nakai that the p-type layer 3 has the front electrode 4 adjacent thereto (see Figs. 1, 4, 6-8 and 11).

On the other hand, a semiconductor layer of Tsuzuki comprises two layers, i.e., a semiconductor layer 802 (i.e., p- or n-type layer) and a semiconductor layer 801 (i.e., n- or p-type layer), laminated in this order from a side that receives light. These two layers thus constitute a p-n junction structure.

It is deemed that the semiconductor layer of Tsuzuki does not need a layer corresponding to the front electrode 4 of Nakai. Namely, the semiconductor layer 802 does not need the adjacent layer corresponding to the front electrode 4 (see Fig. 9).

Therefore, the solar cell of Nakai and the solar cell of Tsuzuki are very different from each other in structure, and accordingly, it is improper to combine the invention of Nakai, in which the p-type layer 3 has the front electrode 4 adjacent thereto by necessity, and the invention of Tsuzuki, in which the semiconductor layer 802 does not need such a layer.

The rejection of claim 1 under 35 U.S.C. §103(a), as allegedly being unpatentable over Nakai in view of Nino et al. (US 5,514,217) and Tsuzuki et al., is respectfully traversed.

The Examiner identified layer 2 in Fig. 11 of Nakai as the claimed first conductivity type semiconductor layer, identified layer 3 as the claimed second conductivity type semiconductor layer, and identified electrode 5 as the claimed front electrode, allegedly being in partial contact with layer 3. Regarding the limitation of implanting second conductivity type impurities into the surface of the first conductivity type semiconductor substrate, the Examiner stated that it is well known in the semiconductor art to implant p-type dopant into the i-type semiconductor layer to obtain p-type semiconductor layer, and referred to Nino as allegedly teaching this (col. 50, lines 3-7). Moreover, regarding the limitation of a partial direct contact between layer 3 and electrode 5, the Examiner recited Tsuzuki, as above.

As discussed above, the combination of Nakai/Tsuzuki fails to teach the claimed "the second conductivity type semiconductor layer being partially in direct physical contact with the front electrode".

The rejection of claim 1 under 35 U.S.C. §103(a), as allegedly being unpatentable over Nakai in view of Nino et al., is respectfully traversed.

The Examiner identified layer 2 (see Fig. 11) as the claimed first conductivity type semiconductor layer, identified 3 as the claimed second conductivity type semiconductor layer, and identified the front electrode 4 as the claimed front electrode being in direct physical contact

with the second conductivity type layer 3. The Examiner asserted, as above, that "although the claim requires a partial direct physical contact between the front electrode and the second conductivity type semiconductor layer, the claim does not preclude the layers being in full contact, and therefore the claim is anticipated", see p. 10 of the Office Action. Moreover, regarding the limitation of the implanting of the first conductivity type semiconductor substrate, the Examiner cited Nino as teaching the limitation.

As discussed above, unlike the Examiner's assertion, "partial" does preclude "full/total", based on plain language interpretation.

The rejection of claims 1 and 8 under 35 U.S.C. §103(a), as allegedly being unpatentable over Schmidt (US 4,577,393) in view of Okamoto et al. (JP 04-356972) and further in view of Matsuyama et al. (US 6,072,117) and Nakayama (US 5,620,530), is respectfully traversed.

Schmidt discloses a method for making a solar cell, according to which a layer 2 acting as a diffusion source is formed on a p-type semiconductor layer 1, for the production of a pn junction in the solar cell. After deposition of layer 3 on layer 2 acting as an AR coating, an annealing process is performed, wherein impurities from the doping layer 2 diffuse into layer 1, thus forming a pn junction 5 within the semiconductor body 1. Subsequently, front side contact 7 is applied, wherein in one embodiment, the contact 7 is entirely alloyed into the AR coating 6 (Figs. 1-5, 7 and col. 4, lines 2-30). Regarding claims 1 and 8, the Examiner, identified layer 1 as the claimed first conductivity type layer, identified layer 4 as the claimed second conductivity type layer which implants second conductivity type impurities into layer 1, and identified the front side contact 7 as the claimed front electrode being partially in direct physical contact with the layer 4, see pp. 12 and 14 of the Office Action. However, the Examiner acknowledged that Schmidt does not disclose the convex/concave portions formed on the surface of the

semiconductor substrate, with the second conductivity type layer becoming thinner as it goes away from the contacted area, and turned to Okamoto for the missing limitation.

Okamoto, cited before, discloses a photoelectric transducer (Fig. 1) comprising a first conductivity type (p-type) semiconductor substrate 10, a second conductivity type (N-type) semiconductor layer 1 formed on the surface of the substrate 10 and being in direct contact with the substrate 10, and a front electrode 5 being in partial direct physical contact with the N-type layer 1, wherein the N-type layer becomes thinner as it goes further from the contacted area.

Moreover, regarding the limitation that the second conductivity type layer and the first conductivity type layer have the convex and concave portions that align with each other, the Examiner cited Matsuyama and Nakayama. Each of Matsuyama and Nakayama discloses a photovoltaic element comprising n-type layer, i-type layer and p-type layer (Fig. 1 in Matsuyama, Fig. 1C in Nakayama), wherein the layers have convex and concave portions that are aligned with each other.

In Schmidt, a semiconductor zone 4 (corresponding to "second conductivity type semiconductor layer 5 of the invention of claims 1 and 8) does not become thinner as it goes farther from an area where the semiconductor zone 4 is partially in direct physical contact with a front side contact 7 (corresponding to "front electrode 8 of the present application), see Fig. 7 in Schmidt.

In Matsuyama, a collecting electrode 108 (corresponding to "front electrode 8 of the invention of claims 1 and 8) does not physically contact with a p-type semiconductor layer 106 (corresponding to "second conductivity type semiconductor layer 5 of the invention of claims 1 and 8) due to a transparent electrode 107 (which is deemed to be an essential element of

Matsuyama) interposed therebetween (see Fig. 1). Therefore, there is no point in replacing the collecting electrode 108 of Matsuyama with a collecting electrode 5 of Okamoto.

A semiconductor layer of Matsuyama comprises three layers, i.e., a p-type semiconductor layer 106 (hereinafter referred to as "p-type layer 106"), an i-type semiconductor layer 105 (i.e., i-type layer), and an n-type semiconductor layer 104 (i.e., n-type layer), laminated in this order from a side that receives light. These three layers thus constitute a p-i-n junction structure.

It is deemed that the semiconductor layer of Matsuyama has the transparent electrode layer 107 on the light-receiving side by necessity. Namely, it is necessary for Matsuyama that the p-type layer 106 has the transparent electrode layer 107 adjacent thereto (see Fig. 1).

On the other hand, a semiconductor layer of Okamoto comprises two layers, i.e., an N-type semiconductor layer 1 (i.e., n-type layer) and a P-type semiconductor substrate 10 (i.e., p-type layer), laminated in this order from a side that receives light. These two layers thus constitute a p-n junction structure.

It is deemed that the semiconductor layer of Okamoto does not need a layer corresponding to the transparent electrode layer 107 of Matsuyama. Namely, the N-type semiconductor layer 1 does not need the adjacent layer corresponding to the transparent electrode layer 107 (see Fig. 1).

Therefore, the solar cell of Matsuyama and the solar cell of Okamoto are very different from each other in structure, and accordingly, it is improper to combine the invention of Matsuyama, in which the p-type layer 106 has the transparent electrode 107 adjacent thereto by necessity, and the invention of Okamoto, in which the N-type semiconductor layer 1 does not need such a layer.

In Nakayama, as is similar to Matsuyama, a collecting electrode 111 (corresponding to "front electrode 8 of the invention of claims 1 and 8) does not physically contact with a p-type a-Si semiconductor layer 109 (corresponding to "second conductivity type semiconductor layer 5 of the invention of claims 1 and 8) due to a transparent electrode 110 (which is deemed to be an essential element of Nakayama) interposed therebetween (see Fig. 1C). Therefore, there is no point in replacing the collecting electrode 111 with the collecting electrode 5 of Okamoto.

A semiconductor layer of Nakayama comprises three layers, i.e., a p-type a-Si semiconductor layer 109 (hereinafter referred to as "p-type layer 109"), an i-type a-Si semiconductor layer 108 (i.e., i-type layer), and an n-type a-Si semiconductor layer 107 (i.e., n-type layer), laminated in this order from a side that receives light. These three layers thus constitute a p-i-n junction structure.

It is deemed that the semiconductor layer of Nakayama has the transparent electrode 110 on the light-receiving side by necessity. Namely, it is necessary for Nakayama that the p-type layer 109 has the transparent electrode 110 adjacent thereto (see Fig. 1C).

On the other hand, the semiconductor layer of Okamoto is as described above.

Therefore, the solar cell of Nakayama and the solar cell of Okamoto are very different from each other in structure, and accordingly, it is improper to combine the invention of Nakayama, in which the p-type layer 109 has the transparent electrode 110 adjacent thereto by necessity, and the invention of Okamoto, in which the N-type semiconductor layer 1 does not need such a layer.

For the above reasons, claims 1 and 8 are allowable.

The rejection of claim 6 under 35 U.S.C. §103(a), as allegedly being unpatentable over Schmidt in view of Uematsu et al. (US 4,916,503) and Okamoto et al. and further in view of Matsuyama et al. and Nakayama, is respectfully traversed.

Amended claim 6 now recites "(d) etching and removing said film serving as a barrier against impurity diffusion". Support for the amendment can be found, for example, p. 13, lines 10-14 of the instant specification. Schmidt does not teach or suggest this feature.

The Examiner identified the forming of a doping layer 2 comprising liquid coating solution as the claimed forming of a film serving as a barrier against impurity diffusion on a first conductivity type layer 1 (Fig. 2 in Schmidt). Moreover, according to the Examiner, Schmidt teaches implanting n-type impurities into the semiconductor substrate 1 through the film 2 to form an n-type layer. The Examiner acknowledged that Schmidt does not teach the substrate having convex and concave portions so that the barrier film becomes thicker from the convex portion to the concave portion, and also that the second conductivity type layer becomes thinner from the convex to the concave portion and turned to Uematsu and Okamoto for these missing limitations.

Uematsu discloses a photoelectric converting device (Fig. 11), wherein the p-type substrate 111 has convex and concave portions, and a front electrode 113 formed on the convex portion (col. 7, lines 40-54). The Examiner then asserted that it would have been obvious to combine Schmidt and Uematsu to form convex and concave portions on the surface of the semiconductor and that since the film 2 of Schmidt comprises a coating solution like the barrier film of the invention, then "the film 2 inherently becomes thicker from the convex portion to the concave portion as the coating solution remains easily in the concave portions", see p. 19 of the

Office Action. Finally, the Examiner cited Okamoto for the limitation of the second conductivity type layer becoming thinner from the convex portions to the concave portions.

The diffusion film 2 in Schmidt is not used as a barrier film against impurity diffusion, since the film 2 itself is the source of the diffusing impurities to the underlying substrate 1. The film 2 remains on top of substrate 1, and after the annealing process it becomes a layer 4 whose conductivity type is opposite to that of substrate 1 (col. 4, lines 2-10). Clearly, layer 2, identified by the Examiner as the claimed barrier film, can not be removed from the device since it comprises the second conductivity type layer.

In contrast, in the invention of claim 6, the barrier film is etched and removed after the diffusion of the impurities to the underlying substrate (p. 13, lines 10-14 in the instant specification). Moreover, none of Uematsu/Okamoto teaches forming a barrier layer on top of a semiconductor layer, so that the barrier layer becomes thicker from the convex to the concave portion.

For the above reasons, claim 6 is allowable.

It is respectfully requested that the rejection of claims 2-5 and 10-11, all dependent from claim 1, also be withdrawn.

In view of the foregoing and other considerations, all claims are deemed in condition for allowance. A formal indication of allowability is earnestly solicited.

The Commissioner is authorized to charge the undersigned's deposit account #14-1140 in whatever amount is necessary for entry of these papers and the continued pendency of the captioned application.

Should the Examiner feel that an interview with the undersigned would facilitate allowance of this application, the Examiner is encouraged to contact the undersigned.

Respectfully submitted,

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